

Application Serial No.: 09/910,684  
Attorney Docket No.: 0190151

**List of Claims:**

1. (Previously Presented) A method comprising:

retrieving a block of pixels associated with a reference block from a reference frame memory; wherein said block of pixels includes NxM pixels wherein N represents the number of pixels in each row of the reference block and wherein M represents the number of pixels in each column of the reference block; and

storing said NxM pixels in a staging memory wherein said NxM pixels are rearranged and stored in the staging memory so as to form P groups each having L pixels such that during each read access cycle all L pixels of a different single one of the P groups is read from the staging memory to a temporary memory; wherein at least one of the P groups of L pixels corresponds to a new row of said block of pixels and at least one of the P groups of L pixels corresponds to a new column of said block of pixels.

2. (Previously Presented) The method of claim 1 wherein said temporary memory is coupled to a processing unit for comparing said block of pixels to a second block of pixels.

3. (Cancelled)

4. (Original) The method of claim 2 wherein said processing unit performs a

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comparison for a motion estimation algorithm.

5. (Currently Amended) The method of claim 1 wherein said staging memory comprises banks of memories, each bank providing a different one of P groups of pixels.

6. (Previously Presented) The method of claim 5 wherein the L pixels of each group is one of a row and column of rearranged pixels.

7. (Previously Presented) The method of claim 1 further comprising providing a search pattern that is executed by loading said temporary memory, in a single cycle, with pixels to provide a next block to be searched.

8. (Previously Presented) The method of claim 7 wherein said search pattern is one of a spiral, horizontal and vertical search pattern.

9. (Currently Amended) The method of claim 1 wherein said rearranging of said pixels comprises reordering said pixels in each row so that ~~each~~ pixels from a single column are spread across a plurality of columns so that they ~~can be~~ are accessed in parallel.

10-11. (Cancelled)

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12. (Currently Amended) An apparatus comprising:

a reference frame memory for storing a block of pixels associated with a reference block; wherein said block of pixels includes  $N \times M$  pixels wherein  $N$  represents the number of pixels ~~in~~ in each row of the reference block and wherein  $M$  represents the number of pixels in each column of the reference block; and;

a staging memory for storing said  $N \times M$  pixels; and

an address translator for rearranging said  $N \times M$  pixels retrieved from said reference frame memory so as to form  $P$  groups each having  $L$  pixels for storing in said staging memory such that during each read access cycle all  $L$  pixels of a different single one of the  $P$  groups is read from the staging memory to a temporary memory; wherein at least one of the  $P$  groups of  $L$  pixels corresponds to a new row of said block of pixels and at least one of the  $P$  groups of  $L$  pixels corresponds to a new column of said block of pixels;

an addressing unit for providing said block of pixels in parallel from said staging memory to said temporary memory.

13. (Cancelled)

14. (Currently Amended) The apparatus of claim 12 wherein said staging memory comprises a plurality of memory banks, each bank providing a different one of said  $P$  groups.

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15. (Previously Presented) The apparatus of claim 12 wherein said staging memory comprises SRAM memory.

16. (Previously Presented) The apparatus of claim 12 wherein said temporary memory is a two-dimensional shift register, and wherein the L pixels in each of the P groups corresponds to a new row or column of said block of pixels.

17. (Previously Presented) The apparatus of claim 12 wherein said temporary memory is coupled to a processing unit for comparing said block of pixels to a second block of pixels.

18. (Original) The apparatus of claim 17 wherein said processing unit performs a comparison for a motion estimation algorithm.

19. (Cancelled)

20. (Previously Presented) The apparatus of claim 16 further comprising:  
a plurality of buffers coupled to said two dimensional shift register for buffering new rows and columns of pixels to be shifted in from the left, right, top and bottom.

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21. (Previously Presented) A method comprising:

retrieving a block of pixels associated with a reference block from a reference frame memory, wherein the block of pixels includes a first plurality of rows of pixels and a second plurality of columns of pixels, wherein the block of pixels further includes a plurality of groups of pixels each having a plurality of pixels; and

storing the pixels of the block in a staging memory in a rearranged form;

wherein, according to the rearranged form, all pixels of any one of the plurality of groups of pixels is read during a single read cycle from the staging memory to a temporary memory, wherein each group of some of the plurality of groups of pixels corresponds to a new row and each group of some other of the plurality of groups of pixels corresponds to a new column.

22. (Previously Presented) The method of claim 21 wherein said rearranged form is such that pixels of one of said new row and new column are stored in the staging memory in a sequential pattern and pixels of the other one of said new row and new column are stored in the staging memory in a non-sequential pattern.

23. (Previously Presented) The method of claim 1 wherein said NxM pixels are rearranged such that pixels of one of said new row and new column are stored in the staging memory in a sequential pattern and pixels of the other one of said new row and new column are stored in the staging memory in a non-sequential pattern.

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24. (Previously Presented) The apparatus of claim 12 wherein said NxM pixels are rearranged such that pixels of one of said new row and new column are stored in the staging memory in a sequential pattern and pixels of the other one of said new row and new column are stored in the staging memory in a non-sequential pattern.